IBM 7340 HYPERTAPE DRIVE

THE IBM 7340 Hypertape Drive (Figure 1) with the IBM 7640 Hypertape Control introduces a new concept in magnetic tape devices. This newest and most advanced magnetic tape system is now available with IBM 7090 Data Processing Systems. Advantages of the 7340 tape system are:

Character Rate: As many as 170,000 alphameric characters or 28,330 words per second.

Reel Capacity: In some applications, more than twice that of 729 IV reels (recorded at high density) even though a reel of 7340 tape is 600 feet shorter.

Cartridge: Machine and file tape reels contained in a sealed cartridge; result is faster loading and unloading of tape without manual threading of the tape.

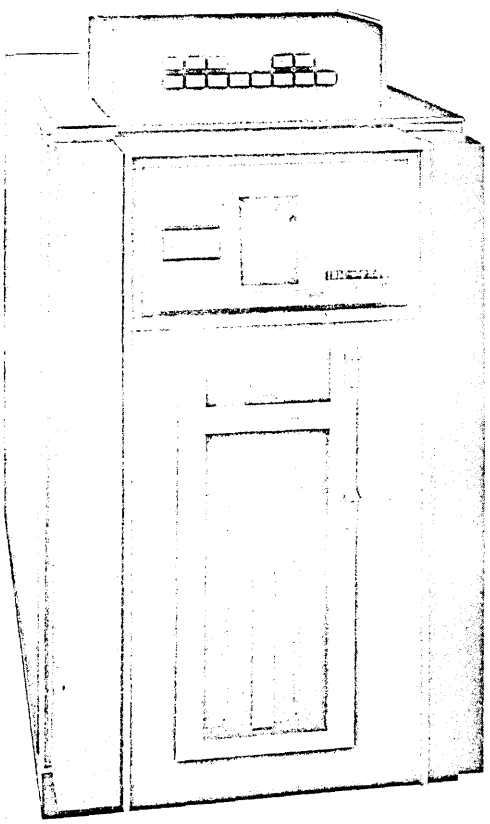


Figure 1. IBM 7340 Hypertape Drive

Read Backward: Allows a recorded tape to be read backward and eliminates necessity of a rewind operation between successive reads of the same recorded tape.

Faster Access: Average access to records in 4.2 milliseconds.

Checking: Automatic detection of all data errors. Automatic correction of all single-bit errors and most double-bit errors.

File Protection: Cartridge file-protect device under program control. Characteristics of the IBM 7340 Hypertape Drive (Figure 1) are shown in Figure 2.

Tape Speed (inches per second)	112.5
Record Density (characters per inch)	1,511
Maximum Data Rate (characters per second)	170,000
Character Time (microseconds per character)	5.9
Average Access Time (in milliseconds)	4.2
Inter-record Gap (length in inches)	0.45

Figure 2. IBM 7340 Hypertape Drive Characteristics.

A tape character consists of the information recorded in a bit-wide column across the ten tracks, perpendicular to the edges of the one-inch tape used by the IBM 7340 Hypertape Drive. When the 7340 is used with the 7090 system, eight of these tracks are used, six for data recording and two for error detection and correction. The remaining two tracks are not used with the 7090 system. Tape track assignments on the 7340 for both BCD and binary codes are shown in Figure 3.

	BCD Code	Binary Code						
Check Bits	C0	C0	C0	C0	C0	C0	C0	Check Bits
	C1	C1	C1	C1	C1	C1	C1	
Not used with 7090	--	--	--	--	--	--	--	Not used with 7090
	--	--	--	--	--	--	--	
Data Bits	B	S	6	12	18	24	30	Data Bits
	A	1	7	13	19	25	31	
	8	2	8	14	20	26	32	
	4	3	9	15	21	27	33	
	2	4	10	16	22	28	34	
	1	5	11	17	23	29	35	

Figure 3. IBM 7340 Hypertape Drive Track Assignment

Complete operational characteristics of both the IBM 7340 Hypertape Drive and IBM 7640 Hypertape Control are in the IBM 7340 Hypertape Drive Reference Manual, Form A22-6616.

A time comparison (in seconds) for 100 records of various character lengths, between the 729 IV at 556 characters per inch and the 7340 at 1,511 characters per inch, is shown in Figure 4.

Characters per Record	729 IV	7340
360	1.30	0.63
720	1.88	0.84
1,800	3.61	1.48
3,600	6.49	2.54

Figure 4. Time Comparison for 100-Record Blocks (in Seconds)

The increased character density of the 7340 also results in more records per reel, even though the total usable tape length on the 7340 is less than that of the 729. Figure 5 compares the capacity of a single reel of tape for the 729 IV (556 characters per inch) and the 7340 (1,511 characters per inch), assuming that 28,440 inches of tape are available for recording with the 729 IV and 21,000 inches of tape are available for recording in the 7340 Hypertape cartridge.

Characters per Record	729 IV	7340
360	20,300	30,500
720	13,900	22,600
1,800	7,100	12,800
3,600	3,900	7,400

Figure 5. Comparison of Single Tape Reel Capacities

The IBM 7340 Hypertape Drive and IBM 7640 Hypertape Control are attached to the IBM 7090 Data Processing System as shown in Figure 6. The IBM 7909 Data Channel

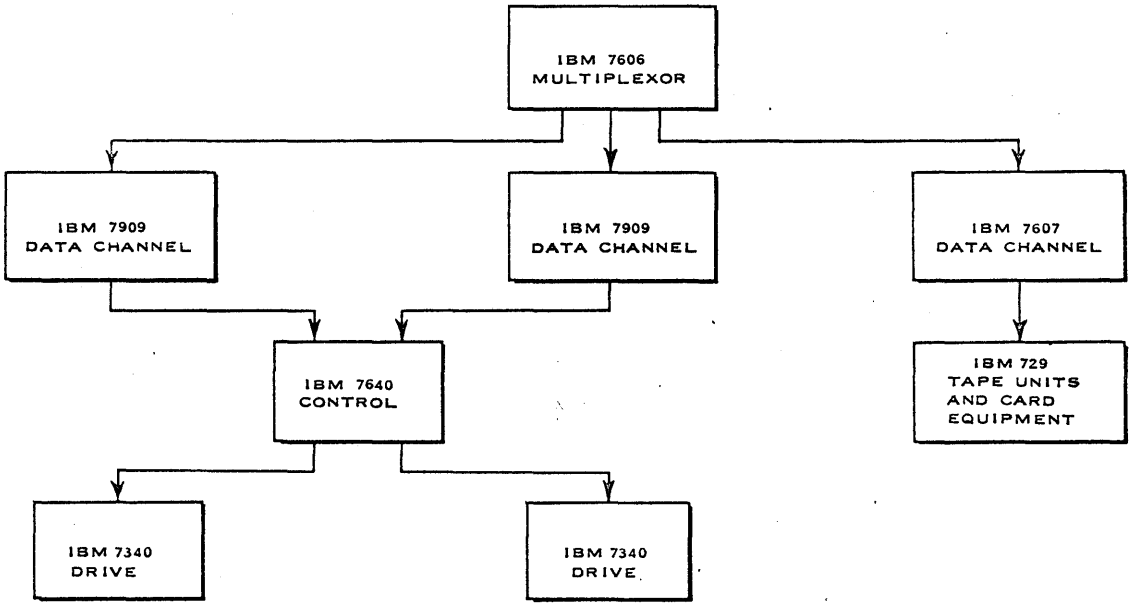


Figure 6. 7090 System Configuration

is a single-channel device while the IBM 7640 Control is a two-channel device. Therefore, simultaneous read-write operation requires that the 7640 be attached to two 7909 data channels. As many as ten 7340 drives may be attached to each channel of the 7640, making a possible total of 20 drives per 7640 control.

HYPERTAPE CARTRIDGE

The cartridge used with the 7340 is shown in Figure 7. The cartridge, plus reels, weighs less than eight and one-half pounds and measures about 17 x 10 x 2 inches. A dust seal protects the magnetic tape from contamination.

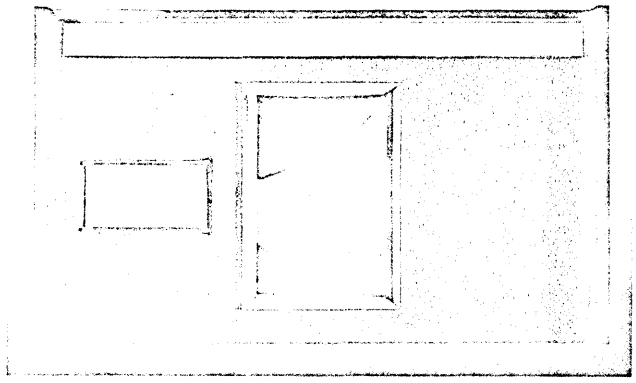


Figure 7. IBM 7340 Cartridge and Reels

The mounting of a cartridge is shown in Figure 8. Loading and threading of tape occur automatically after the operator mounts the cartridge and presses the load key on the drive. Tape does not move backward to the beginning of tape (BOT) marker until the operator presses the rewind key on the drive or until the computer initiates a rewind control operation under program control. Less than 15 seconds are required to load and thread tape.

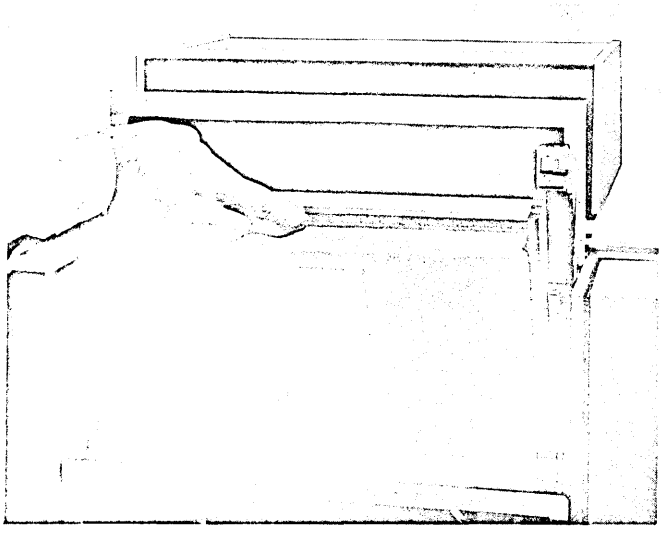


Figure 8. IBM 7340 Cartridge Mounting

TAPE MOTION AND MARKERS

A single capstan moves the tape forward or backward at 112.5 inches per second. Rewinding occurs at 225 inches per second with tape in the vacuum columns.

Three markers appear on the tape to set off the recording area from the physical ends. About 25 feet from the physical beginning of tape is a marker called the beginning of tape (BOT). The BOT is adjacent to the machine edge of the tape.

About 25 feet from the physical end of tape is another marker called the end of tape (EOT). The EOT is the same size as the BOT but is located midway between the edges of tape. Tape motion stops immediately when the machine detects the EOT.

Because the 7340 cannot move tape forward past the EOT, a third marker, called the end warning area (EWA) marker precedes the EOT on tape by about 40 feet. The EWA marker is located adjacent to the edge of tape nearest the operator. When tape is being written, detection of the EWA does not stop tape motion but signals the end-of-tape condition.

OPTIONAL FEATURES

Two optional features are available for use on the IBM 7909 Data Channel.

Read Backward Character Assembly and Storage: Facilitates processing of data received from a recorded tape being read in a backward direction by assembling the characters in reverse order.

BCD Translation Feature: Accomplishes binary-to-BCD character translation for magnetic tapes prepared or to be used by other IBM data processing systems employing IBM 7340 Hypertape Drives.

SYSTEM INSTRUCTIONS AND COMMANDS

INFORMATION FLOW

Data being transmitted between core storage and the 7340 pass through the 7640 control, IBM 7909 Data Channel, and the IBM 7606 Multiplexor. Operation of the data channel is initiated in the CPU. Once started, the channel operates independently of the main program being executed by the CPU. The data channel has the responsibility for controlling quantity and destination of all data transmitted between core storage and the 7340.

Programs for a channel operation are stored in core storage just as are instructions executed by the central processing unit. To distinguish between a main (CPU) program and a channel program, data executed by a data channel are termed commands, data executed by the CPU are termed instructions and data executed by the 7640 control are termed orders.

DATA FLOW

A simplified flow chart, containing 7909 data channel registers and data switches concerned with data flow, is shown in Figure 9.

1. Storage Bus In and Storage Bus Out: These 36-position data switches direct data between the multiplexor and the data register of the 7909 data channel.

2. Data Register: This 36-position register serves as a buffer register for data flowing between core storage and the assembly register.

Normal data channel and central processing unit operations are not discussed in this bulletin. Description of these operations are in the IBM 7090 Data Processing System Reference Manual, Form A22-6528.

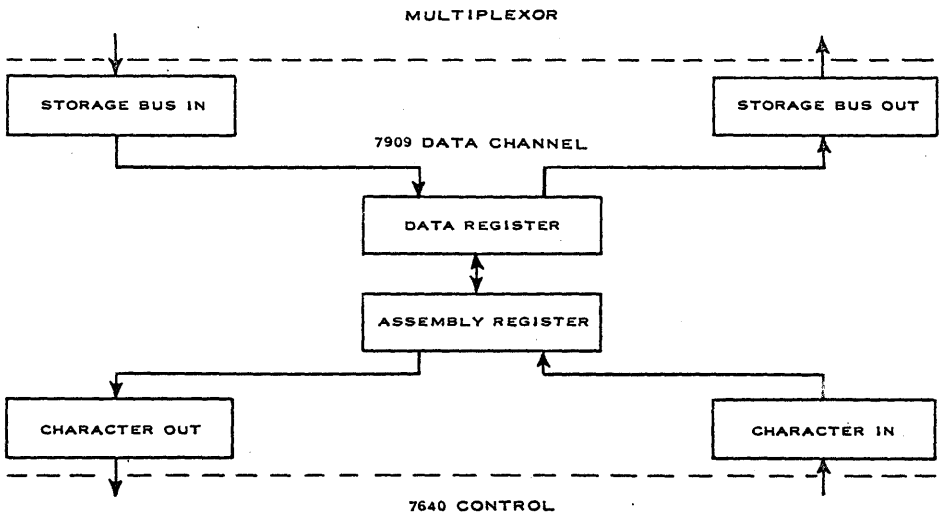


Figure 9. Data Flow within the IBM 7909 Data Channel

3. Assembly Register: The 36-position assembly register assembles characters from the character-in switch and, when six characters have been assembled, sends them (as a word) to the data register. A word from the data register is placed in the assembly register and then sent, one character at a time, to the character-out switch. Characters placed in or taken from the assembly register are automatically shifted (in the register) to take their proper sequence in the word.

4. Character Out and Character In: These six-position data switches direct data (by character) to or from 7340 drives.

OPERATION AND CONTROL INFORMATION FLOW

Four additional 7909 data channel registers are used to decode and control channel operations (Figure 10). These registers are:

Operation Register and Decoder: This five-position register (positions S, 1, 2, 3, and 19) hold the operation code of the command being executed by the data channel. Decoding circuitry receives operation bits of word locations and sets up switching circuits for the execution of the command.

Address Counter: The address counter (15 positions) is used to locate data addresses in core storage. On operations under word count control, the address counter is increased by one for each word transmitted. Storage words are thus taken from or placed into sequential word locations. The counter is normally set from the address portion of the command effecting the data transfer.

Word Counter: The 15-position word counter is used to control the number of words to be transmitted. As each word is transmitted, the word counter is reduced by one. A signal is given when the contents of the word counter are reduced to zero. The word counter is normally set from the count portion of the command effecting the data transfer.

Command Counter: This 15-position counter locates and controls the sequence of commands taken from core storage.

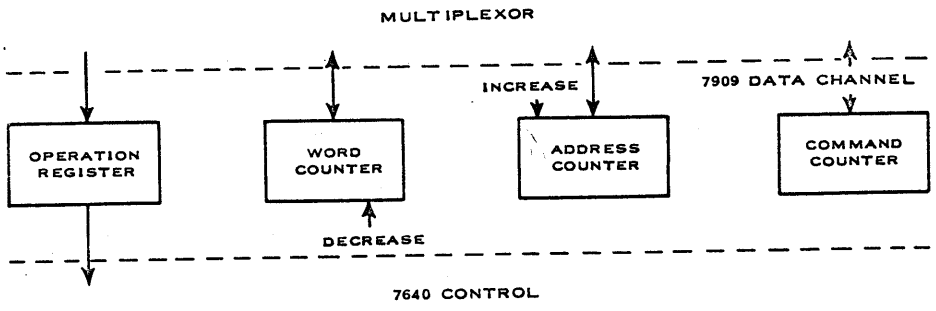


Figure 10. Operation and Control Registers of IBM 7909 Data Channel

CENTRAL PROCESSING UNIT INSTRUCTIONS

The format used in the following descriptions of instructions and commands uses the established formats contained in the IBM 7090 Data Processing System Reference Manual, Form A22-6528. Execution timing is not included since execution is dependent on organization of commands in storage and the status of the data channel when it is addressed. Symbols used are:

C = Count Field
F = Indirect Address Flag
T = Index Register Action
Y = Address Field

RSCA--Reset and Start Channel A

The channel is selected and reset, and takes its next command from address Y. The instruction is interlocked against channel activity; if the instruction is executed while the channel is busy, its execution is delayed until the channel is in wait status.

Instruction	Code	Name
RSCB	-0540	Reset and Start Channel B
RSCC	+0541	Reset and Start Channel C
RSCD	-0541	Reset and Start Channel D
RSCE	+0542	Reset and Start Channel E
RSCF	-0542	Reset and Start Channel F
RSCG	+0543	Reset and Start Channel G
RSCH	-0543	Reset and Start Channel H

STCA--Start Channel A

If the channel is not in wait status, execution of this instruction is delayed. If in wait status, the channel is started and takes its next command from the address part of the wait command

Instruction	Code	Name
STCB	-0544	Start Channel B
STCC	+0545	Start Channel C
STCD	-0545	Start Channel D
STCE	+0546	Start Channel E
STCF	-0546	Start Channel F
STCG	+0547	Start Channel G
STCH	-0547	Start Channel H

SCHA--Store Channel

Execution of this instruction causes the specified channel to be selected and that channel's command counter contents to be placed in positions 21-35 of location Y. The channel's address counter contents are placed in positions 3-17 of location Y. Positions S, 1, 18, and 19 are reserved for diagnostics and their contents cannot be predicted.

Instruction	Code	Name
SCHB	-0640	Store Channel B
SCHC	+0641	Store Channel C
SCHD	-0641	Store Channel D
SCHE	+0642	Store Channel E
SCHF	-0642	Store Channel F
SCHG	+0643	Store Channel G
SCHH	-0643	Store Channel H

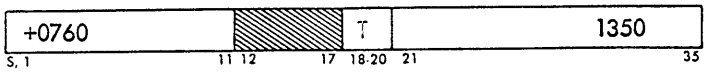
ENB--Enable from Y

When this instruction is executed, the contents of location Y determine which signals may cause a trapping operation. Execution of each enable instruction cancels the effect of previous enable instructions. The channel may be disabled (traps will not occur) by executing an enable instruction whose operand contains a zero in the proper position. Trapping signals are controlled as follows:

Signal Due to	Channel	Effective if a "1" in
Control word	A	0035
Control word	B	0034
Control word	C	0033
Control word	D	0032
Control word	E	0031
Control word	F	0030
Control word	G	0029
Control word	H	0028

Execution of a trap inhibits all further traps until a new enable instruction is executed or a restore-channel-traps instruction is executed. Depression of the reset or clear key, or execution of an RIC instruction, also disables all channels.

RICA--Reset Channel A



This instruction, when executed by the central processing unit, causes all conditions in the channel to be reset. This instruction is not interlocked against channel activity.

If data transmission is taking place when a RIC occurs, validity of the data already transmitted cannot be guaranteed.

Instruction	Code	Name
RICB	0760-- 2350	Reset Channel B
RICC	0760-- 3350	Reset Channel C
RICD	0760-- 4350	Reset Channel D
RICE	0760-- 5350	Reset Channel E
RICF	0760-- 6350	Reset Channel F
RICG	0760-- 7350	Reset Channel G
RICH	0760--10350	Reset Channel H

INPUT-OUTPUT COMMANDS

CTL--Control

The control command is decoded in the channel itself. Information contained in address Y is sent to the 7640 control, starting with the high-order character, and continues until an end signal is received from the control. If more than one word location is necessary to transmit all of the data required by the channel, the next word is taken from location Y + 1, etc. This process continues until an end signal is received; the next command is then taken from the storage location following the control command.

CTLR--Control and Read

This command causes the channel to transmit control information in the same manner as for a control command, and prepares the channel to read. When an end signal is received from the 7640 control (signalling the end of the order), the channel proceeds to the next command in sequence. When a copy command is encountered, the channel is placed in read status and data are transmitted to storage under control of the copy.

CTLW--Control and Write

This command causes the channel to transmit control information in the same manner as for a control command, and prepares the channel to write. When an end signal is received from the 7640 control (signaling end of order) the channel proceeds to the next sequential command. When a copy command is encountered, the channel is placed in write status and data are transmitted from storage to the 7640 control under control of the copy command.

SNS--Sense

This command prepares the channel for a sense operation and then proceeds to the next sequential command. When a copy command is encountered, the channel places the 7640 control in sense status and information is sent to storage under control of the copy command.

CPYD--Copy and Disconnect

This command, when decoded by a channel not in read or write status, causes a sequence check and thus a channel interrupt. If the channel is in read or write status, this command causes C words to be transmitted between the channel and core storage, starting with location Y. Data transmission continues until C is reduced to zero or an end signal is received by the channel. In either event, the channel read or write select is reset. If, while a CPYD is being executed, an end signal is received before the count is reduced to zero, the channel read or write select is reset and the channel obtains a new command from the next sequential location.

If the next command is other than a copy, the channel executes that command. If the next command is a copy, the channel interrupts on a program sequence check. The last word transmitted under CPYD control remains in the channel assembly register.

If the count for a CPYD goes to zero before the end signal is received, the channel does not get the next sequential command until an end or unusual-end signal is obtained.

In general, when operating under CPYD control, the channel does not obtain the next sequential command until either an end (or unusual end signaling an error) occurs. In the event of an unusual end, an interrupt occurs.

CPYP--Copy and Proceed

This command, when decoded by a channel not in read or write status, causes a sequence check and channel interrupt. If the channel is in read or write status, this command causes C words to be transmitted between the channel and storage starting with location Y. End signals from the 7640 control are ignored and data transmission continues until C is reduced to zero.

When C is reduced to zero, the channel does not disconnect but obtains the next sequential command. If this command is either a CPYD, CPYP, or TCH, operation is normal and data transmission resumes. If the new command is other than CPYD, CPYP, or TCH, the channel disconnects and interrupts on a sequence error.

CHANNEL INTERRUPT AND CONTROL COMMANDS

The channel interrupts command sequence if either the attention or unusual-end conditions occur. The attention interrupt will, in general, be delayed until after the end signal is generated. If attention is generated while the channel is in wait status, the

interrupt starts the channel. This interrupt stores the location counter contents in a fixed storage location and transfers channel control to another fixed location. Return to the original channel sequence by means of a leave interrupt program (LIP) command again causes the channel to be in wait status. Interrupt locations are:

Channel	Store Command Counter	Obtain Next Command
A	0042	0043
B	0044	0045
C	0046	0047
D	0050	0051
E	0052	0053
F	0054	0055
G	0056	0057
H	0060	0061

Conditions which yield a channel interrupt may be readily handled by a special channel program sequence. Thus, in the case of either unusual-end or attention signals, the channel is capable of diagnosing the more elementary problems and responding accordingly. As the last input-output unit selected remains selected, the problem of determining which unit on a channel is being dealt with is eliminated. Conditional transfer commands (TCM) can then be used to diagnose the problem, corrective action can be taken, and either a LIP or indirect TCH command can be executed to return to the original channel command sequence.

Once an interrupt occurs on a given channel, subsequent attempts to interrupt on the channel are inhibited until a LIP command is executed by the channel. This command, when executed by a given channel, causes that channel to take its next command from the fixed address contained in the fixed location into which that channel's location counter contents were stored when the interrupt occurred. If a trap command occurs in the interrupt program, it is processed in the normal fashion. Interrupts are also inhibited if a trap is being executed by the channel. This inhibiting persists until either a reset and start or start channel instruction (depending on whether the channel was enabled or not) is executed by the central processing unit. See "TWT."

TCH--Transfer in Channel

This command is the transfer command for all channels. When a TCH command is executed, command sequence control is transferred to location Y.

WTR--Wait and Transfer

When this command is decoded, the channel stops operation and may be thought of as waiting. The channel location counter contains the location of the WTR command. When the channel is told to start, it takes its next command from the location specified by the address part of the WTR command. If an interrupt occurs while the channel

is in wait status, return from the interrupt program (by means of the LIP command) puts the channel back in wait status.

TWT--Trap and Wait

Upon decoding a TWT command, the channel suspends operation until either a reset and start or start channel instruction is given by the CPU, depending upon conditions described below. If the channel is enabled for control word or end-of-file traps, the channel causes the CPU to trap to a fixed location. Particulars concerning this trap are described in the "Data Channel Trap" section of the IBM 7090 Data Processing System Reference Manual, Form A22-6528.

If the channel is enabled, start channel instructions are ignored until the trap is executed or a reset and start channel is given, resetting the trap condition. If the channel is not enabled, either a reset and start or a start channel resets the trap and causes the channel to resume operation.

Channel interrupt signals are remembered but not executed until the channel brings in a command other than the TWT. (An RSC resets these stored interrupt signals.)

After the channel has stopped operation as a result of a TWT, the channel command counter contains the location of that command.

Assume that B is the location where the instruction counter contents are stored when a trap occurs on this particular channel and that CPU control is transferred to B + 1. SUB is the entry point for the subroutine that the channel requests the CPU to execute.

Command	Address
XMT	B+1, 1
TRA	SUB
TWT	Y

TCM--Transfer on Condition Met

When the count (C) field is not zero, this command causes C to specify one of the six characters in the assembly register for comparison against the mask field (M). If a bit-for-bit comparison is achieved, the channel executes a transfer to location Y. If the comparison is not achieved, the channel proceeds to the next sequential command.

If C is zero, the channel check condition register is compared against M. Transfer conditions for the comparison are the same as above. When indirect addressing is used, control is transferred to the indirectly addressed location when the condition is met.

Unless interrupts are inhibited, the channel interrupts whenever a bit appears in one or more positions of the channel's condition register. The register indications are:

Position	Function
1	I-O Check: This condition occurs when the channel fails to obtain a storage cycle in time to satisfy the demands of the attached I-O device. The condition is also monitored in the CPU.
2	Sequence Error: This condition occurs as a result of an improper sequence of commands.
3	Unusual End: This condition occurs when transmission is terminated by an unusual-end rather than a normal end signal.
4	Attention (Channel 1): This is a signal indicating a change in the status of an I-O device attached to the 7909 channel.
5	Not used.
6	Read-Write Check: This condition occurs when the 7640 is not operational and a command is encountered by the channel, or when the character rate of the I-O device exceeds the capability of the channel.

All interrupts are executed immediately following the logic termination of the command during which they occur. Attention interrupts occurring during a read or write operation are executed following the termination of that operation. The SMS command allows inhibiting of attention and unusual end interrupts individually; interrupts may be all disabled by forcing an interrupt and not executing a LIP command.

TDC--Transfer and Decrement Counter

Upon execution of this command, the contents of the six-bit channel control counter are examined. If the contents are not zero, the counter is decremented by one (one is subtracted from it) and control is transferred to location Y. If the contents of the counter are zero, the channel proceeds to the next sequential command without disturbing the counter.

SMS--Set Mode and Select

Execution of this command causes the contents of positions 30-35 of this command to set or reset specific status indicators as follows:

Bit	Function
30*	Read backward
31*	BCD mode
32	Inhibit unusual end signals
33	Inhibit attention signals

* Optional Features

In all cases, the presence of the bit causes the status indicator to be set and the functions to be enabled, while the absence of the bit resets the status indicator and disables the function. Machine and power-on resets also reset the status indicators.

An insert control counter (ICC) command, with a count of zero, places the status indicators into the sixth character position of the assembly register. With indirect addressing, the SMS command status indicators are set or reset with bits 30-35 of the location specified by bits 21-35 of the command. After executing the SMS command, the channel proceeds to the next sequential command.

Read Backward Character Assembly and Storage Optional Feature: When an order to select for backward reading is executed, and position 30 of a previously executed set mode and select command contains a bit, characters received from the 7640 are assembled by the data channel in reverse order.

BCD Translation Optional Feature: When position 31 of the SMS command contains a bit, each BCD character transmitted by a subsequent copy command is changed as follows:

From I-O Device		To Storage	
B A	8 4 2 1	B A	8 4 2 1
0 0	0 0 0 0	1 1	0 0 0 0
0 0	1 0 1 0	0 0	0 0 0 0
0 1	x x x x	1 1	x x x x
1 1	x x x x	0 1	x x x x
1 0	zones do not change		

From Storage		To I-O Device
0 0	0 0 0 0	0 0 1 0 1 0
1 1	0 0 0 0	0 0 0 0 0 0
0 1	x x x x	1 1 x x x x
1 1	(not zero)	0 1 x x x x
1 0	zones do not change	
0 0	(not zero)	No Change

ICC--Insert Control Counter

When count (C) is not zero, this command causes the C field to specify one of the six characters in the assembly register to be replaced by the contents of the control counter. The remaining five characters are not affected. If C is zero, the sixth character of the assembly register is replaced by the contents of the set mode and select status indicators. In either case, the channel proceeds to the next sequential command after execution of the ICC.

LCC--Load Control Counter

This command causes the contents of the channel control counter to be replaced by the six low-order positions of the count field of the LCC command. The channel then proceeds to the next sequential command. If the LCC is indirectly addressed (bit in position 18), the contents of the control counter are replaced by the six low-order bits contained in the location specified by positions 20-35 of the LCC.

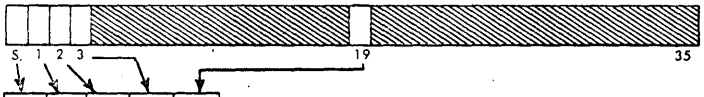
XMT--Transmit

The transmit command causes the C words immediately following the location of the XMT command to be transmitted to C locations starting at location Y.

When the count (C) field is reduced to zero and the Cth word has been transmitted, the channel obtains its next command from the location of the XMT command plus C, plus one. If the initial count field is zero, the XMT command is skipped and the channel proceeds to the next sequential command.

The transmission rate is dependent upon a variety of factors, including the number of channels attached to the system.

Input-Output Command Bit Configurations



S	1	2	3	19	
0	1	0	0	0	Control
0	1	0	0	1	Control and Read
0	1	0	1	0	Control and Write
0	1	0	1	1	Sense
0	1	1	0	0	Load Assembly Register
0	1	1	0	1	Store Assembly Register
0	1	1	1	0	Trap and Wait
1	1	0	0	0	Set Mode and Select
1	1	0	0	1	Leave Interrupt Program
1	1	0	1	0	Transfer and Decrement Counter
1	1	0	1	1	Load Control Counter
0	0	0		0	Wait and Transfer
0	0	0		1	Transmit
0	0	1		0	Transfer in Channel
1	0	0		0	Copy and Proceed
1	0	1		0	Copy and Disconnect
1	0	1		1	Transfer on Condition Met
1	1	1		1	Insert Control Counter

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